Fig. 1

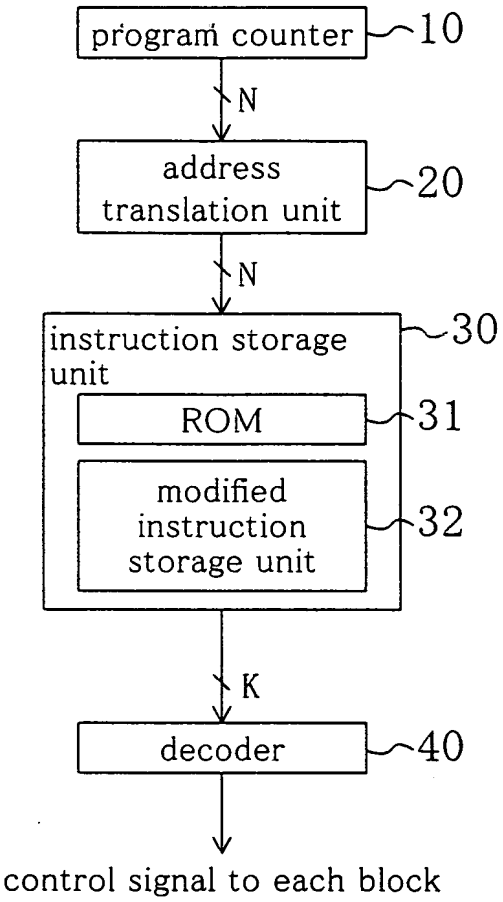
program counter
10
N
address translation unit
20
N
instruction storage unit
30
ROM
31
modified instruction storage unit
32
K
decoder
40
control signal to each block

Fig. 2

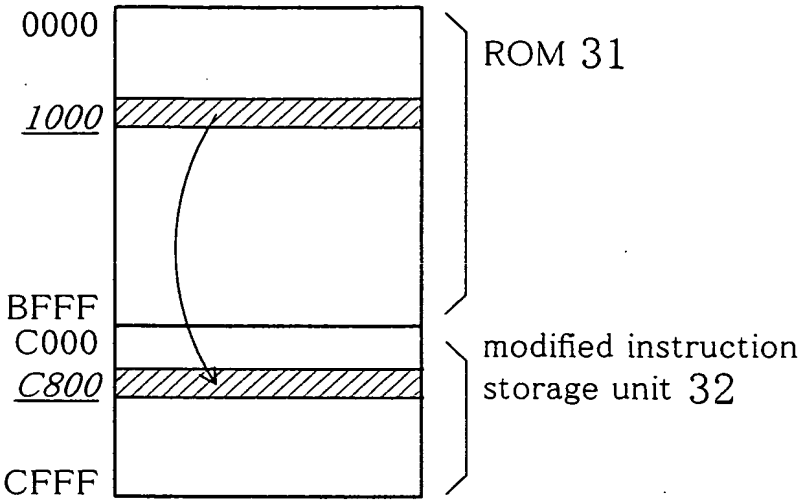
0000
1000
BFFF
C000
C800
CFFF
ROM 31
modified instruction
storage unit 32

Fig. 3

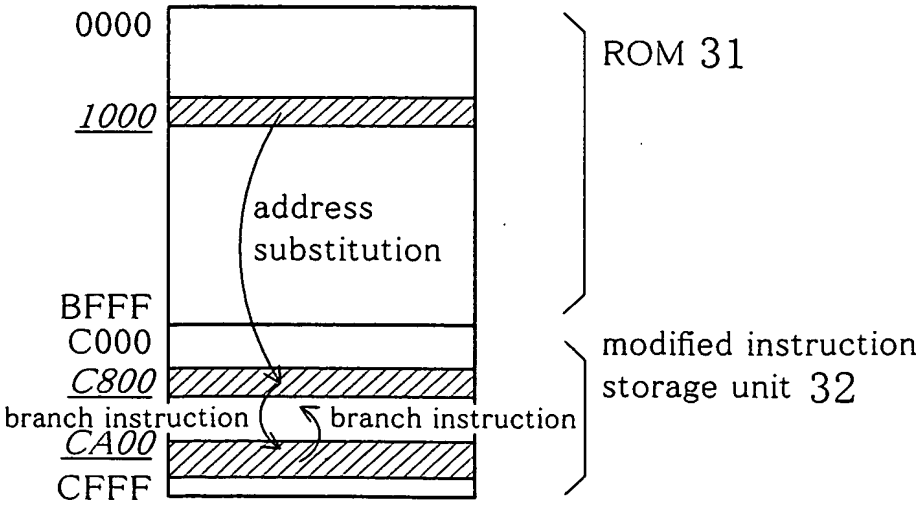
0000
1000
address
substitution
BFFF
C000
C800
branch instruction
branch instruction
CA00
CFFF
ROM 31
modified instruction
storage unit 32

Fig. 4

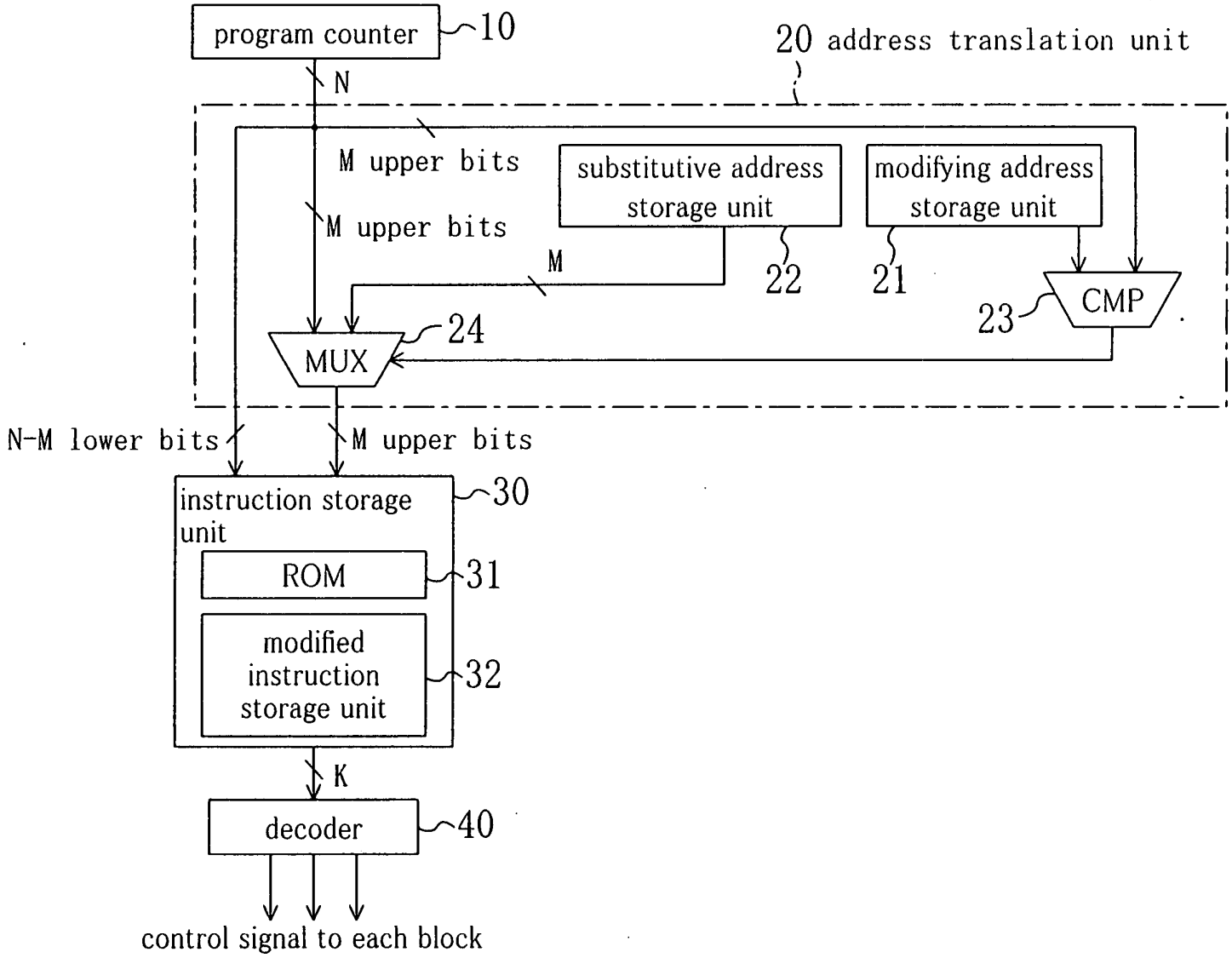
program counter
10
20 address translation unit
N
M upper bits
substitutive address storage unit
modifying address storage unit
M upper bits
M
22
21
CMP
23
24
MUX
N-M lower bits
M upper bits
instruction storage unit
30
ROM
31
modified instruction storage unit
32
K
decoder
40
control signal to each block

Fig. 5

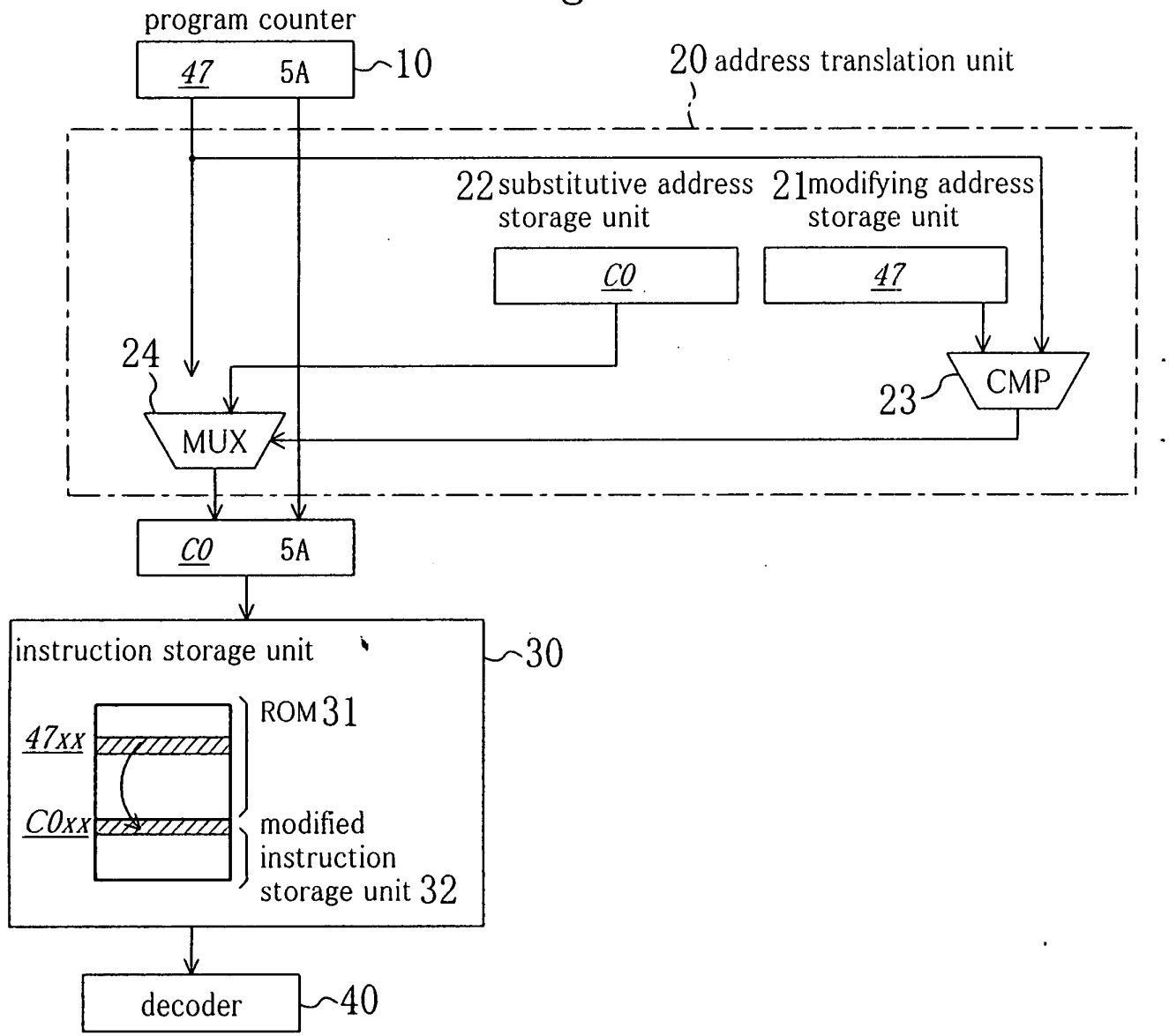
program counter
47
5A
10
20 address translation unit
22 substitutive address storage unit
21 modifying address storage unit
C0
47
24
MUX
23
CMP
C0
5A
instruction storage unit
30
47xx
C0xx
ROM 31
modified instruction storage unit 32
decoder
40

Fig. 6

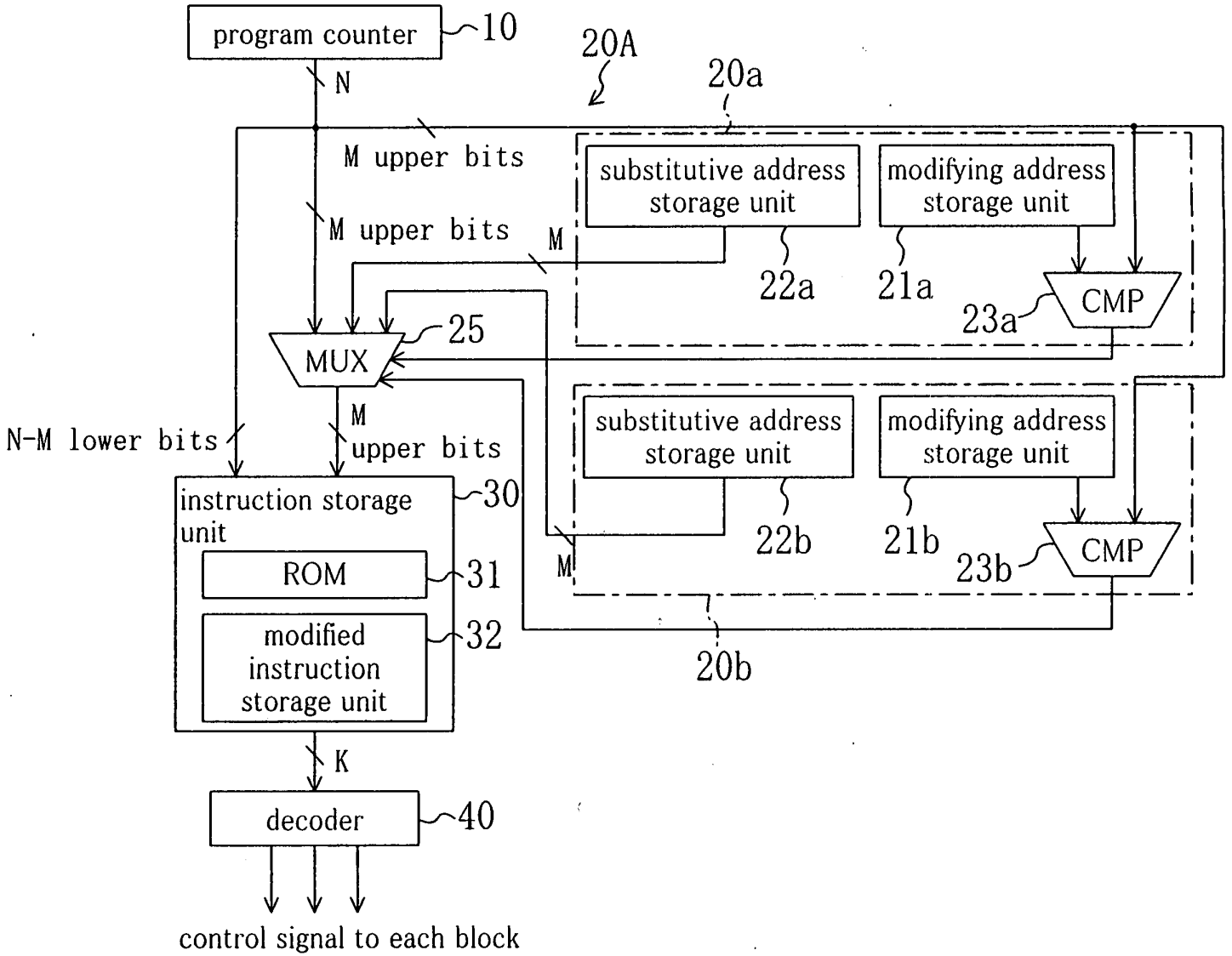
program counter
10
20A
20a
N
M upper bits
M upper bits
M
substitutive address storage unit
modifying address storage unit
22a
21a
CMP
23a
25
MUX
M
upper bits
N-M lower bits
substitutive address storage unit
modifying address storage unit
22b
21b
CMP
23b
M
instruction storage unit
30
ROM
31
modified instruction storage unit
32
20b
K
decoder
40
control signal to each block

Fig. 7

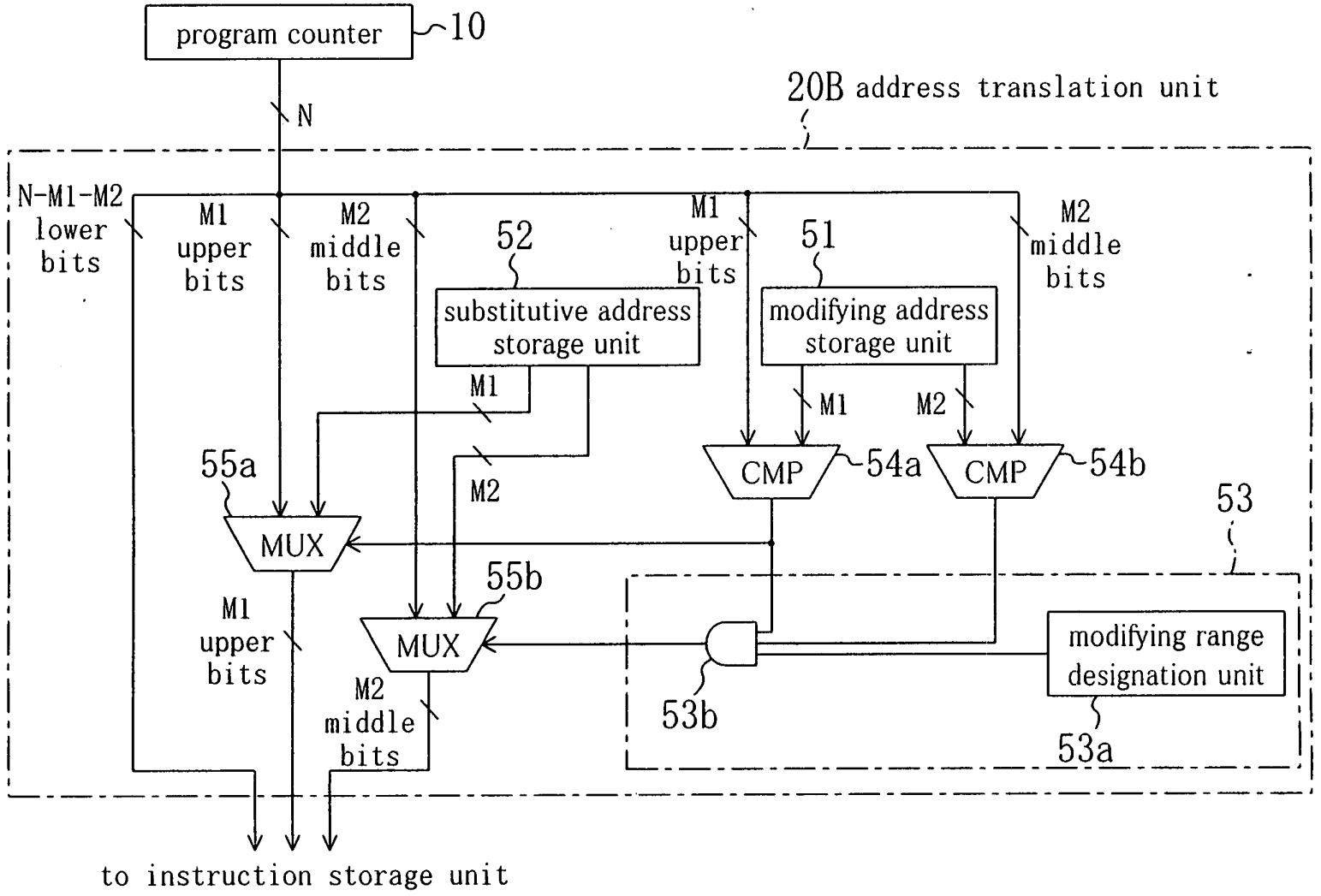
program counter
10
20B address translation unit
N
N-M1-M2 lower bits
M1 upper bits
M2 middle bits
52
substitutive address storage unit
M1 upper bits
51
modifying address storage unit
M2 middle bits
M1
M2
55a
MUX
CMP
54a
CMP
54b
53
55b
MUX
M1 upper bits
M2 middle bits
modifying range designation unit
53b
53a
to instruction storage unit

Fig. 8

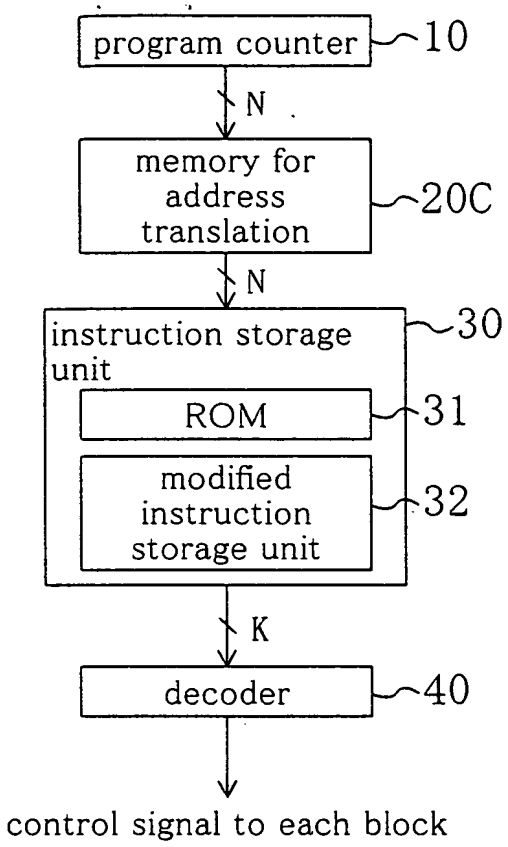
program counter
10
N
memory for address translation
20C
N
instruction storage unit
30
ROM
31
modified instruction storage unit
32
K
decoder
40
control signal to each block

Fig. 9

| input address | output address |
|---|---|
| 00 | 00 |
| 01 | 01 |
| ⋮ | ⋮ |
| 47 | C0 |
| ⋮ | ⋮ |

Fig. 10

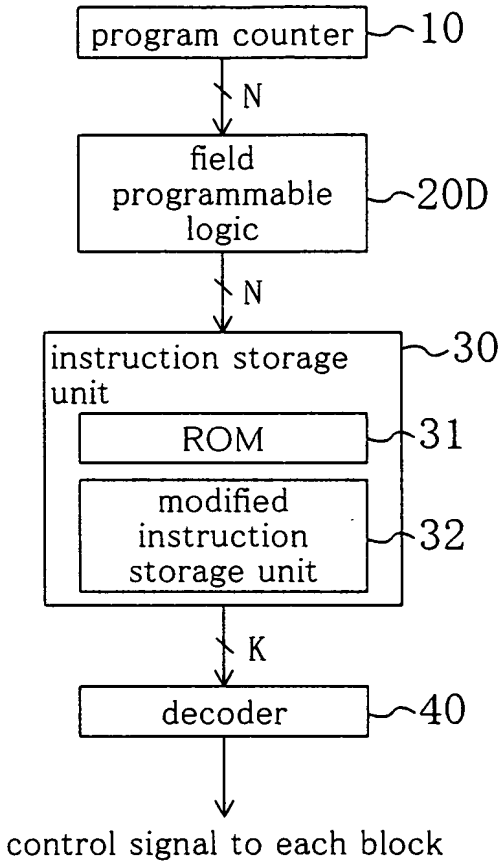
program counter
10
N
field programmable logic
20D
N
instruction storage unit
30
ROM
31
modified instruction storage unit
32
K
decoder
40
control signal to each block

Fig. 11
PRIOR ART

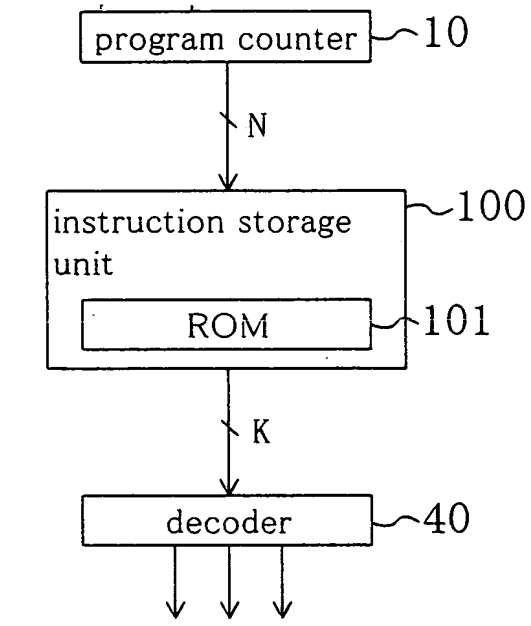

Fig. 12
PRIOR ART